REMARKS

The foregoing amendments are responsive to the February 2, 2009 Office Action. Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks.

Response to Rejection of Claims 3-4, 7-8 and 23-26 Under 35 U.S.C. 102(b)

The Examiner rejected Claims 3-4, 7-8 and 23-26 under 35 U.S.C. 102(b) as being anticipated by Davies et al. (U.S. Patent No. 6,329,846). Davies teaches a charging circuit 401 that receives an input clock signal and charges precharge nodes 405, 406 during a first phase of the clock signal. The cross connected shunt transistors 410 and 411 are provided to hold one of the outputs during a second phase of the clock signal. The charge discharge operation of the logic gate is driven by the clock signal. The gate does not propagate the precharge signal, rather the precharge signal must be provided by the clock.

By contrast, Applicants teach and claim logic providing a pre-discharge wave wherein the differential input signals, which are the outputs of preceding dynamic gates, pre-charge (or pre-discharge) the gate. There is no need to force the output signals to '1' or `0`. Consequently, performing the predischarge operation inside the gate is redundant and can be omitted. The pre-charge or pre-discharge wave is propagated from the logic outputs of one stage to the logic inputs of the next stage.

Regarding Claim 3, the cited prior art does not teach or render obvious a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, the differential logic cell configured to propagate a pre-discharge wave.

Regarding Claim 4, the cited prior art does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a pre-discharged logic cell configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 7, the cited prior art does not teach or render obvious a wave dynamic differential logic wherein a differential logic cell transmits a precharge value generated by a precharge generator.

Claims 23-26 depend, directly or indirectly, from Claim 3 and recite additional patentable limitations over and above those of Claim 3.

Accordingly, Applicants assert that Claims 3-4, 7-8 and 23-26 are allowable over prior art, and Applicants request allowance of Claims 3-4, 7-8 and 23-26.

Response to Rejection of Claims 5-6 and 9-12 Under 35 U.S.C. 103(a)

The Examiner rejected Claims 5-6 and 9-12 under 35 U.S.C. 103(a) as being unpatentable over Davies et al. in view of Forbes (U.S. Patent No. 6,437,604). Davies is discussed above. Like Davies, Forbes teaches that the precharge operation of the logic gate 100 is driven by the clock signal Phi. The gate does not propagate the precharge signal as a precharge wave, rather the precharge signal must be provided by the clock.

Regarding Claim 5, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to generate a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 6, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 9, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to transmit on a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 10, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a differential dynamic logic register configured to generate a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 11, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to transmit on a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 12, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Accordingly, Applicants assert that Claims 5-6 and 9-12 are allowable over prior art, and Applicants request allowance of Claims 5-6 and 9-12.

No Disclaimers or Disavowals

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Co-Pending Applications of Assignee

Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

Docket No.	Serial No.	Title	Filed
UCLARF.002NP	10/554,763	System for Biometric Signal Processing With Hardware and Software Acceleration	August 7, 2006
UCLARF.003NP	10/565551	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	September 11, 2006
UCLARF.003DV1	12/191,144	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	August 13, 2008
UCLARF.008NP	12/092,687	Methods and Apparatus for Context-Sensitive Telemedicine	May 5, 2008

Summary

Applicants respectfully assert that Claims 1-26 are in condition for allowance, and Applicants request allowance of Claims 1-26. If there are any remaining issues that can be resolved by a telephone conference, the Examiner is invited to call the undersigned attorney at (9449) 721-6305 or at the number listed below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: May 7, 2009

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